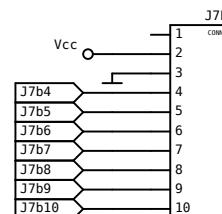
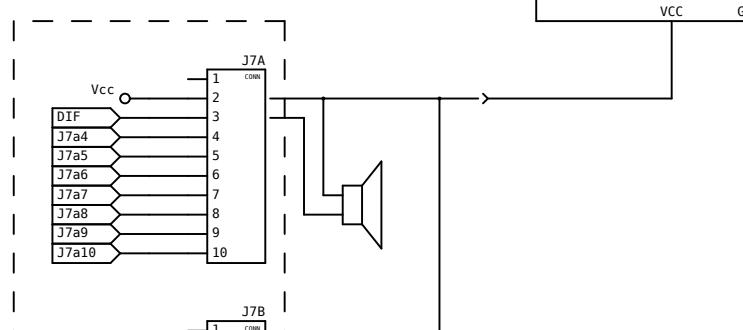
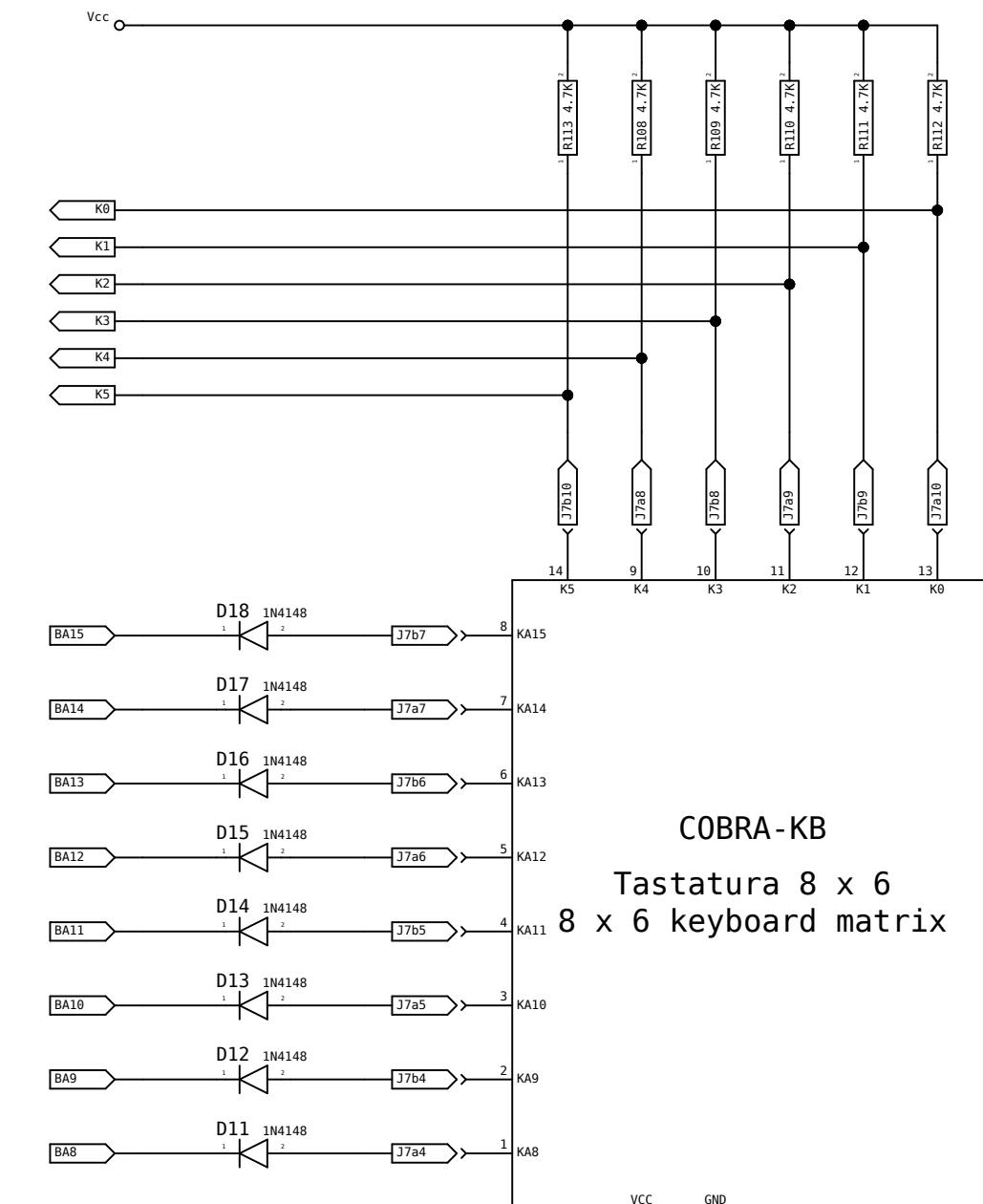


TITLE μC CoBra - Arbitrul de memorie si logica de comanda
CoBra μC - Memory access prioritizer and command logic

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 1 OF 16	DRAWN BY: ElectroNNix



J7A+B - conector tastatura

J7A+B - keyboard connector

TITLE μC CoBra - Circuitul de conectare tastatura
CoBra μC - Keyboard interfacing circuit

FILE: CoBra

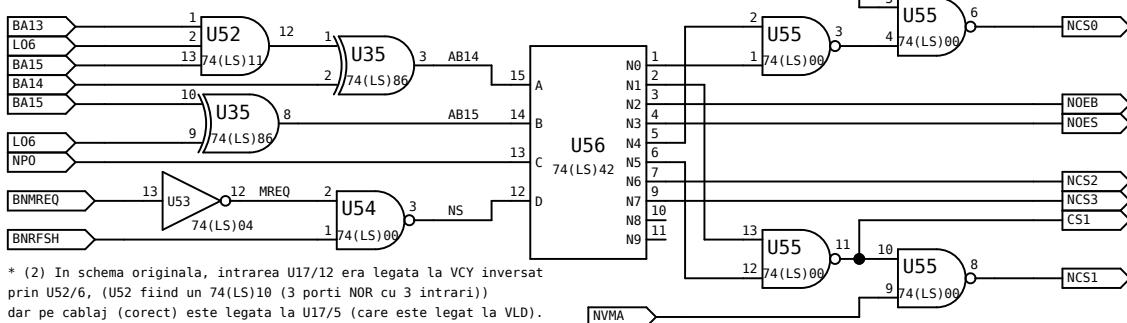
REVISION: 3 (original design, 64KB DRAM)

PAGE 2 OF 16

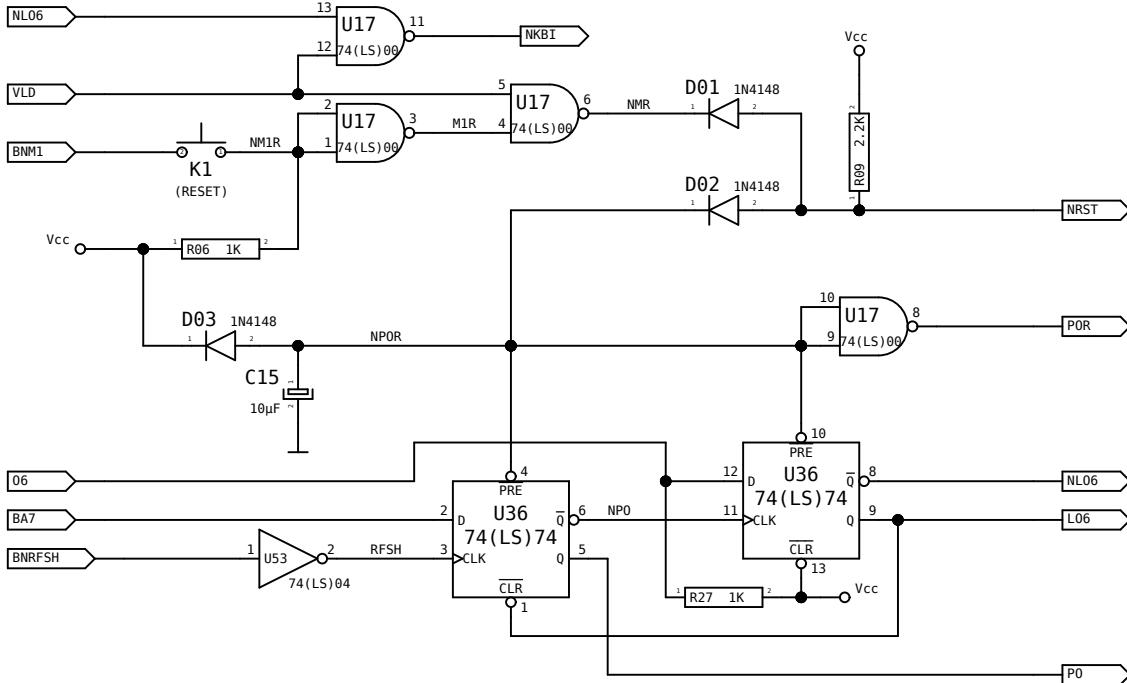
DRAWN BY: ElectroNNix

* (1) In schema originala, U52 era un 74(LS)10 (3 porti NOR cu 3 intrari), BA13, BA15 si L06 erau trecute prin U52/12,1,2,13 si apoi iesirea U52/12 era inversata prin poarta U52/8,9,10,11 folosita ca inversor, care mai departe era legata la U35/1. Pe cablajul original, U52 are portile (3,4,5,6) si (8,9,10,11) nefolosite (pinii lasati in gol) iar iesirea U52/12 este legata direct la intrarea U35/1. Considerind cablajul corect, singura optiune este ca U52 sa fie un 74(LS)11, adica 3 porti OR cu cete 3 intrari, iar poarta (3,4,5,6) nu mai e necesara conform notei de mai jos, ca si poarta (8,9,10,11).

* (1) In the original schematics, U52 was a 74(LS)10 (3 NOR 3-input gates), BA13, BA15 and L06 were passed through U52/12,1,2,13 and then the output U52/12 was inverted through gate U52/8,9,10,11 used as inverter, which was further connected to U35/1. On the original mainboard, U52 has the gates (3,4,5,6) and (8,9,10,11) unused (N.C. pins) and output U52/12 is connected directly to U35/1. Assuming the mainboard is correct, the only option is for U52 to be a 74(LS)11, i.e. 3 OR 3-input gates, and gate (3,4,5,6) is no longer required according the note below, just as gate (8,9,10,11).



* (2) In the original schematics, input U17/12 was connected to VCY inverted through U52/6, (U52 being a 74(LS)10 (3 NOR 3-input gates)) but on the original mainboard (correctly) it is connected to U17/5 (which is connected to VLD).

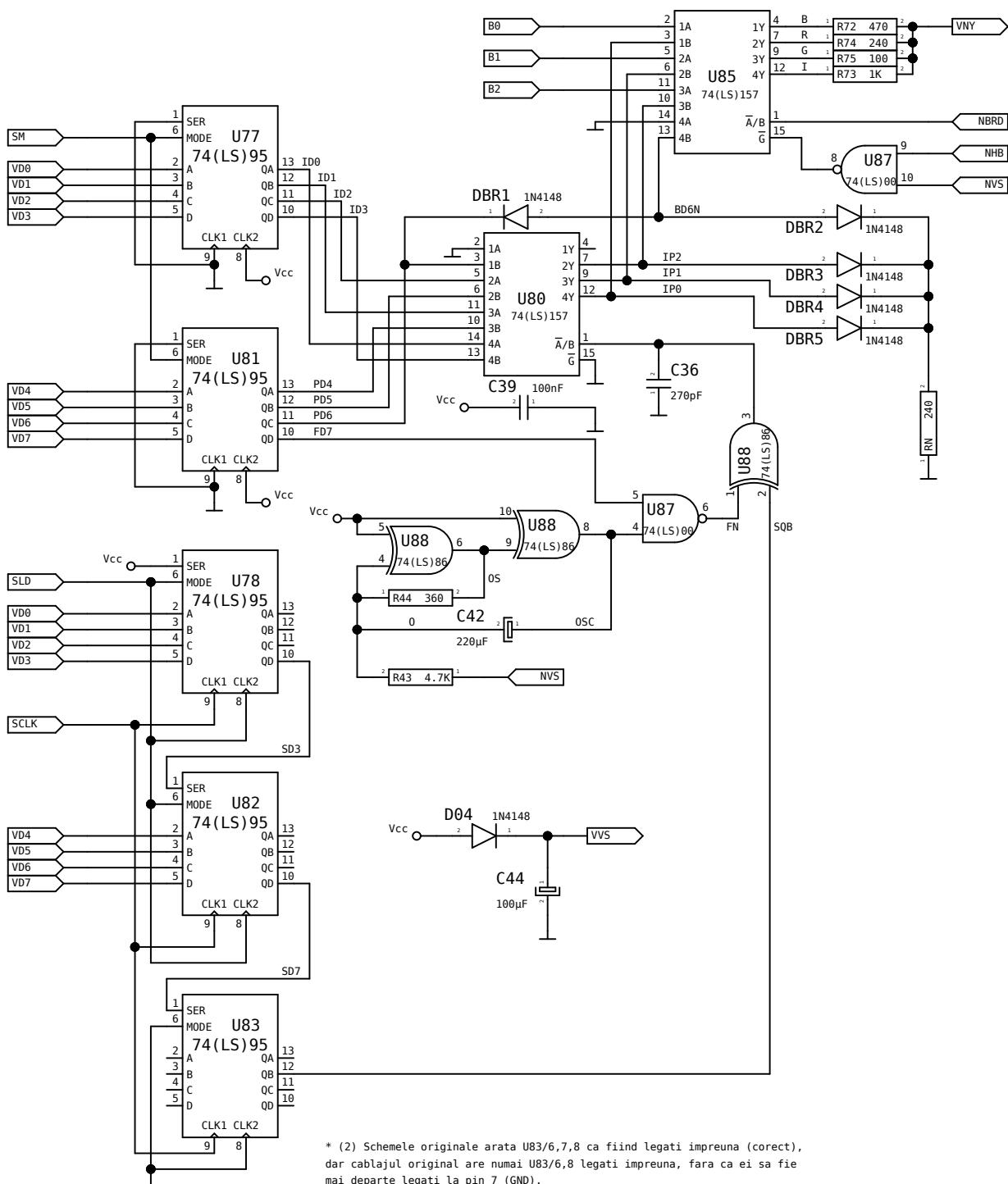


TITLE µC CoBra - Circuitul de configurare si selectie
CoBra µC - Configurator and selector circuit

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 3 OF 16	DRAWN BY: ElectroNNix

* (1) In schema originala, diodele DBR1-5 si rezistenta RN sunt desenate (cu toate ca diodele nu sunt denumite) dar pe cablajul original nu sunt prevazute, iar U85/13 este legat direct la U80/3. Ca urmare, cablajul original nu permite functia de BRIGHT. Am modificat cablajul adaugand gauri pentru DBR1-5 si RN si intrerupind deci legatura directa dintre U85/13 si U80/3.

* (1) In the original schematics, diodes DBR1-5 and resistor RN are drawn (although the diodes don't have names) but on the original mainboard they are not placed, and U85/13 is directly connected to U80/3. Therefore, the original mainboard would not allow the BRIGHT function. I have modified the mainboard layout by adding mounting holes for DBR1-5 and RN and therefore interrupting the direct connection between U85/13 and U80/3.

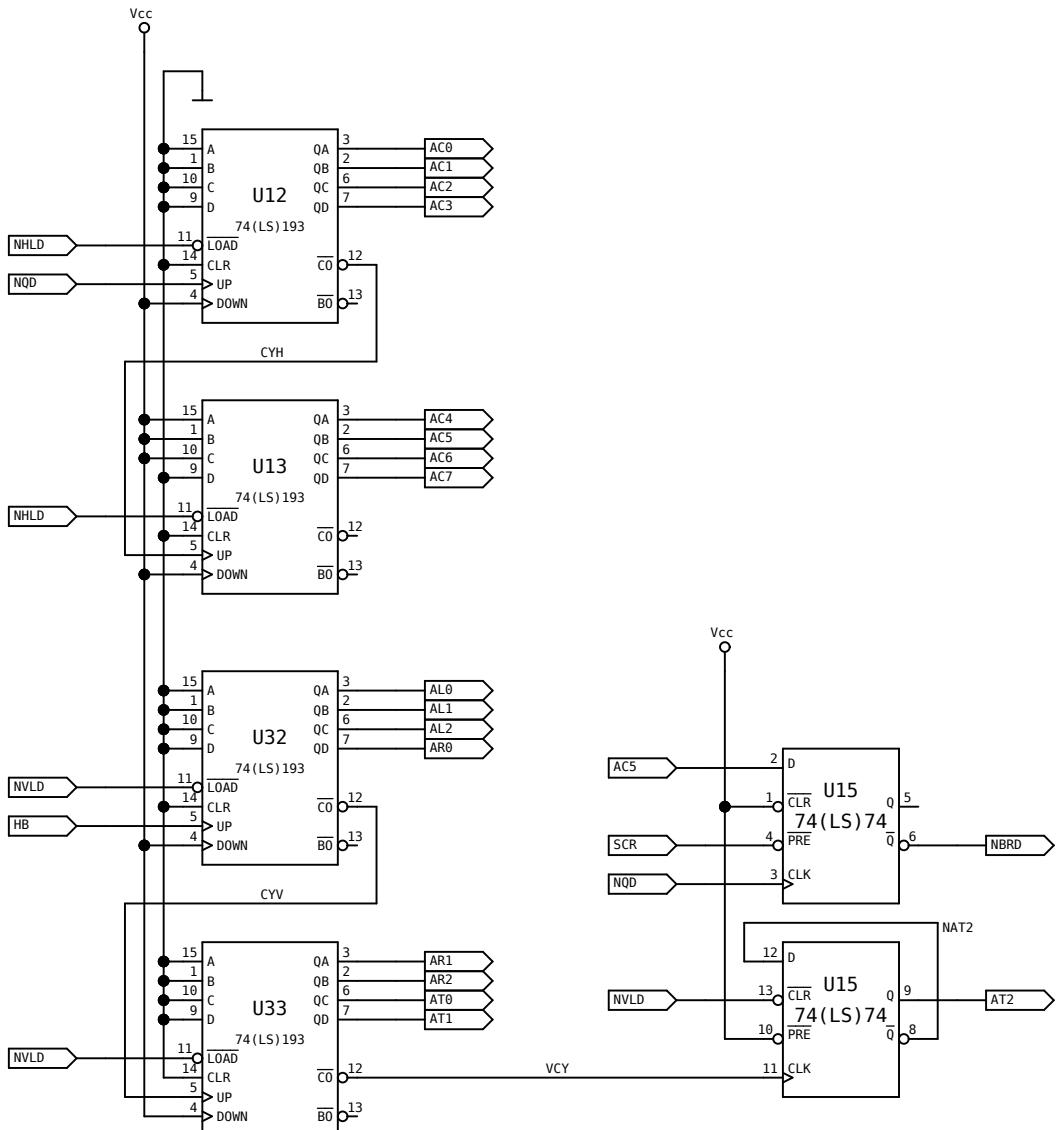


* (2) Schemele originale arata U83/6,7,8 ca fiind legati impreuna (corect), dar cablajul original are numai U83/6,8 legati impreuna, fara ca ei sa fie mai departe legati la pin 7 (GND). Am modificat cablajul placii de baza pentru a corespunde schemei originale. (Vezi legatura #25 fata 2)

* (2) The original schematics show U83/6,7,8 connected together (correctly), but the original mainboard layout only has U83/6,8 connected together without them being further connected to pin 7 (GND). I have modified the mainboard layout to match the original schematics. (See rewiring #25 side 2)

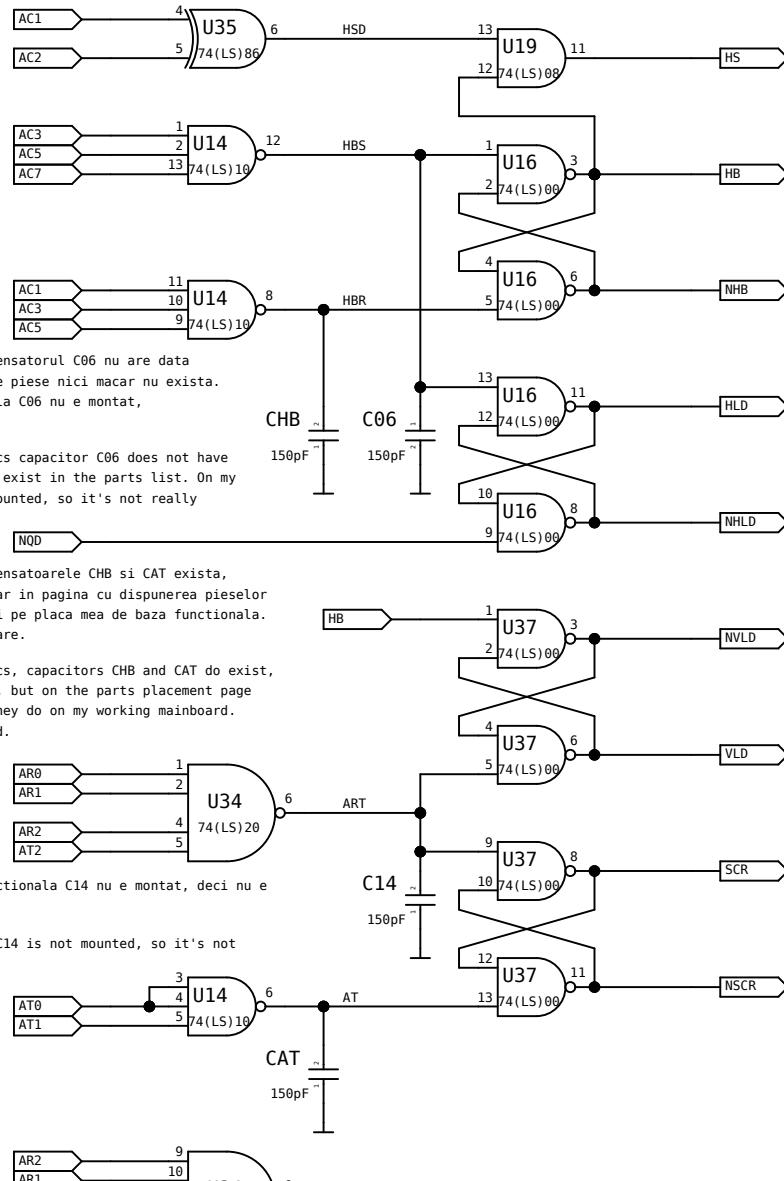
TITLE	μC CoBra - Circuitul formator semnal video CoBra μC - Video signal generator circuit		
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FILE:	CoBra	REVISION:	3 (original design, 64KB DRAM)
PAGE	4 OF 16	DRAWN BY:	ElectroNNix



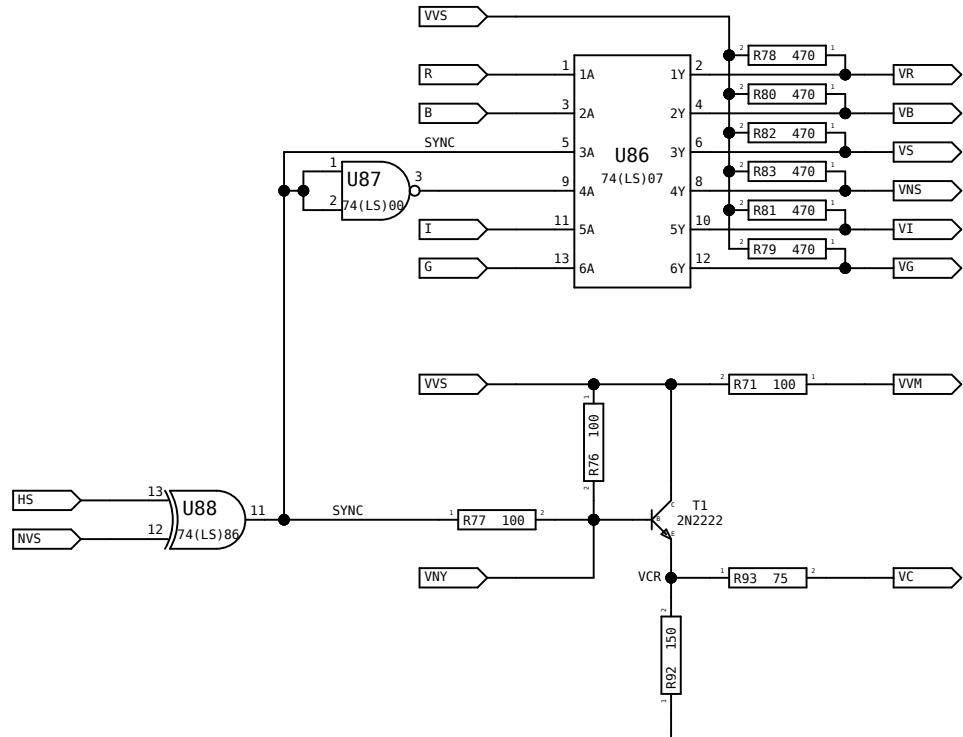
TITLE **μC CoBra - Circuitul de generare adrese video**
CoBra μC - Video address generator circuit

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 5 OF 16	DRAWN BY: ElectroNNix

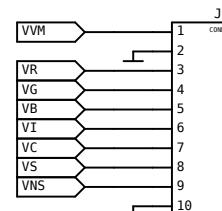


TITLE μC CoBra - Circuitul generator de sincroimpulsuri
CoBra μC - Video sync pulses generator circuit

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 6 OF 16	DRAWN BY: ElectroNNix



J1 - CONECTOR VIDEO
J1 - VIDEO CONNECTOR



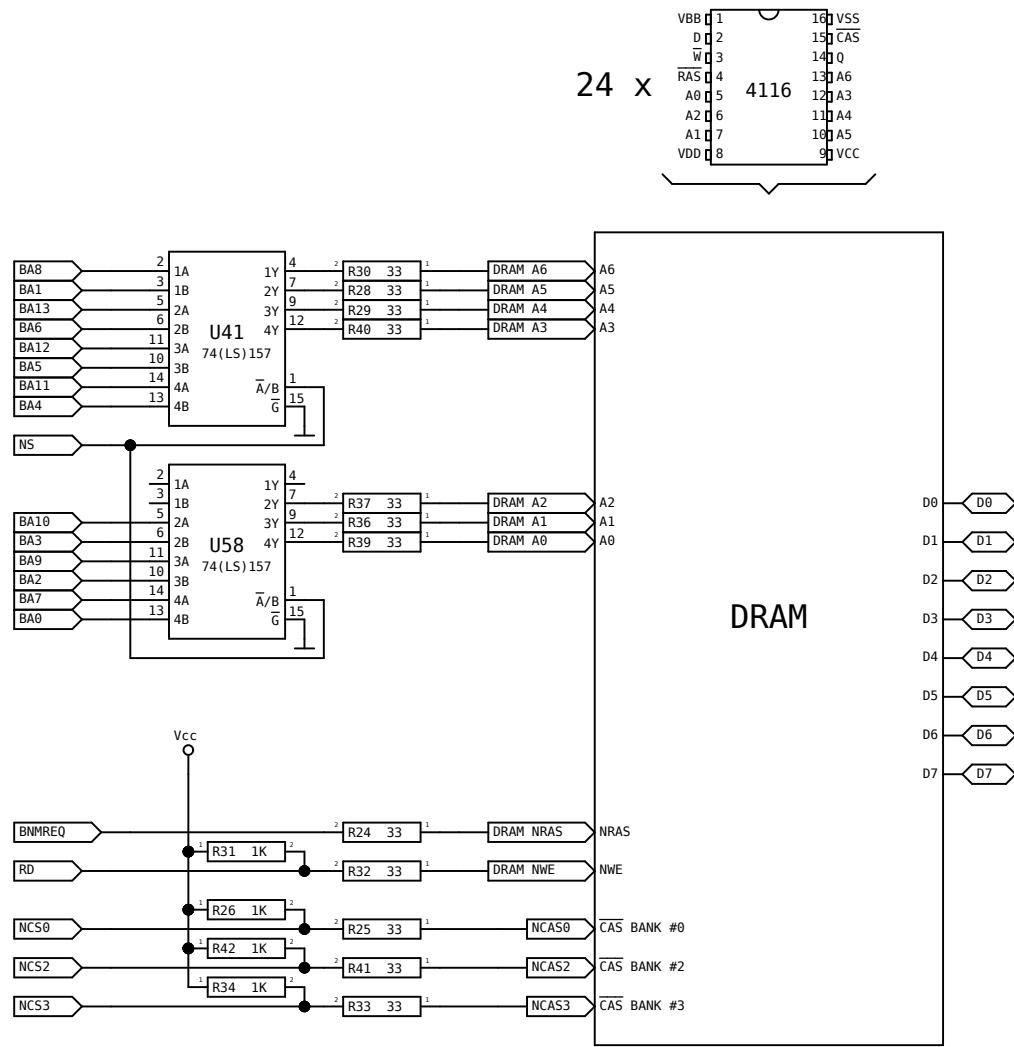
TITLE **μ C CoBra - Circuitul de interfata cu monitorul TV**
CoBra μ C - TV monitor interfacing circuit

FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

PAGE 7 OF 16

DRAWN BY: ElectroNNix



TITLE **μ C CoBra - Circuitul memoriei dinamice - pag.1/2**
CoBra μ C - Dynamic memory circuit - pag.1/2

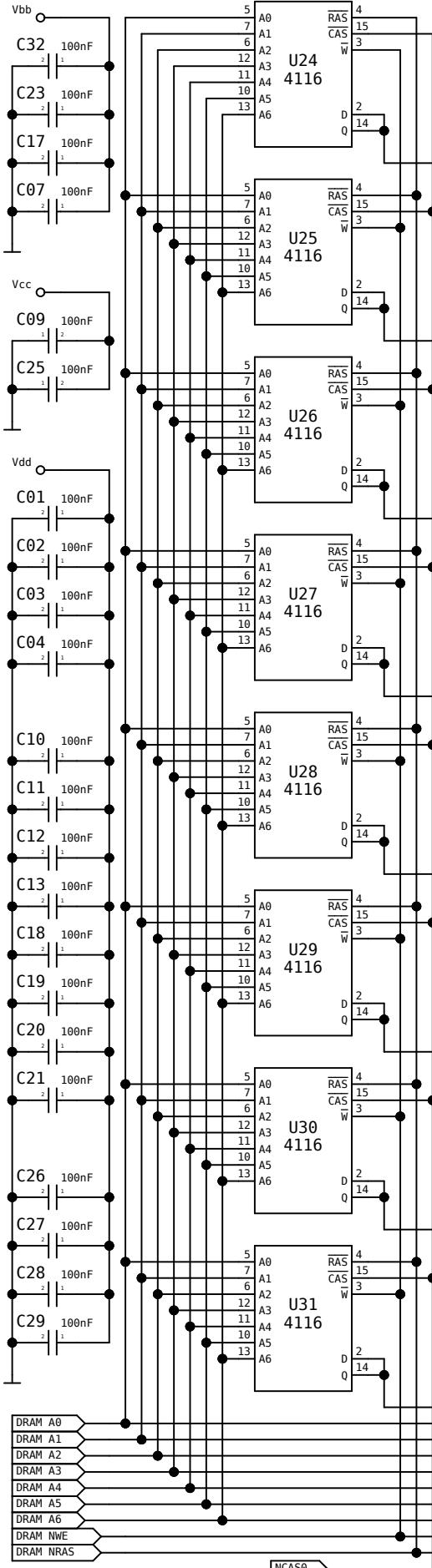
FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

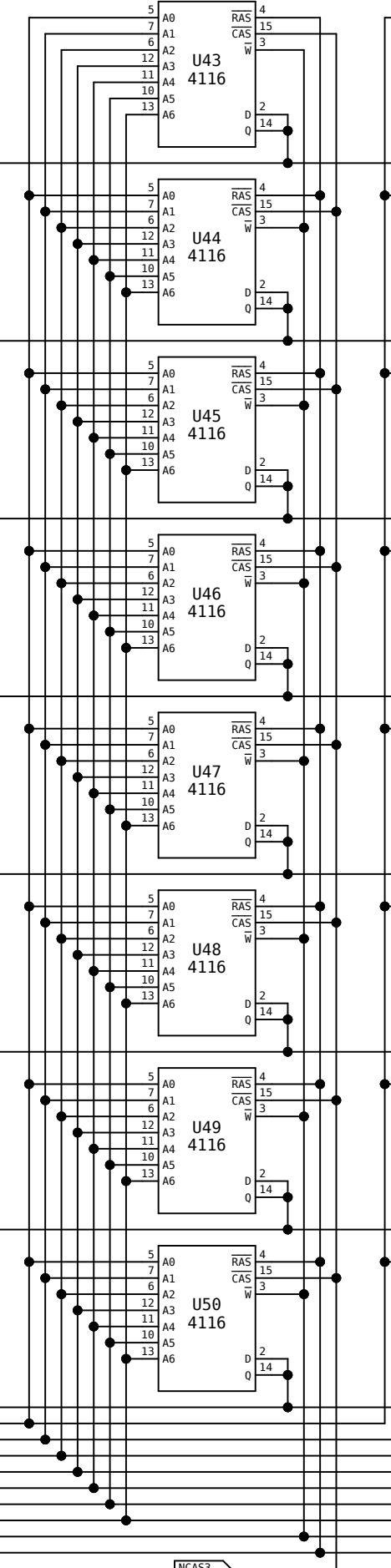
PAGE 8 OF 16

DRAWN BY: ElectroNNix

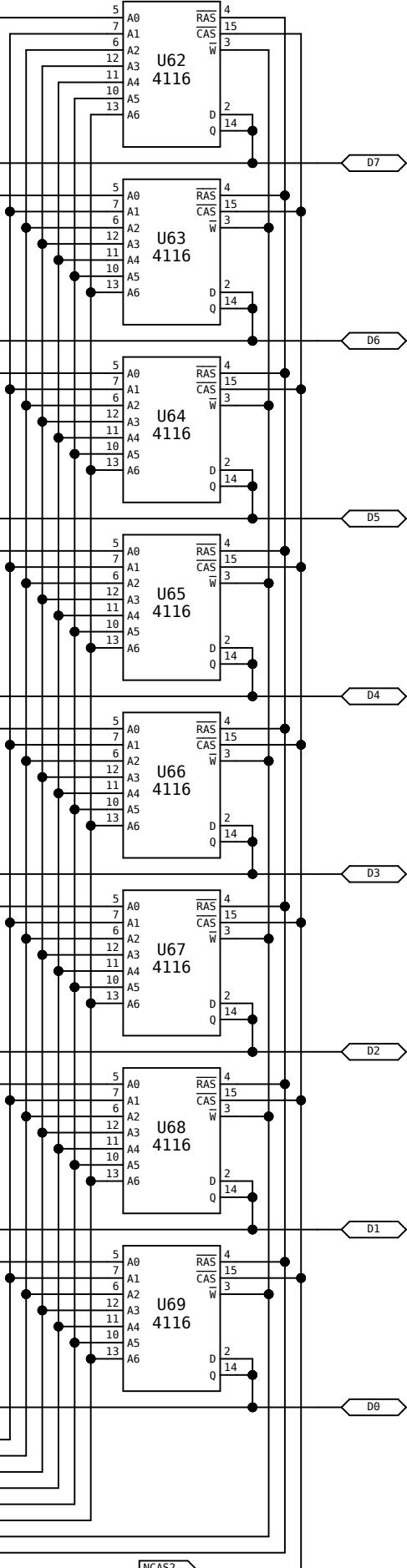
DRAM #0



DRAM #3



DRAM #2



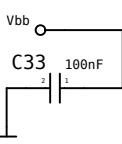
TITLE **μ C CoBra - Circuitul memoriei dinamice - pag.2/2**
CoBra μ C - Dynamic memory circuit - pag.2/2

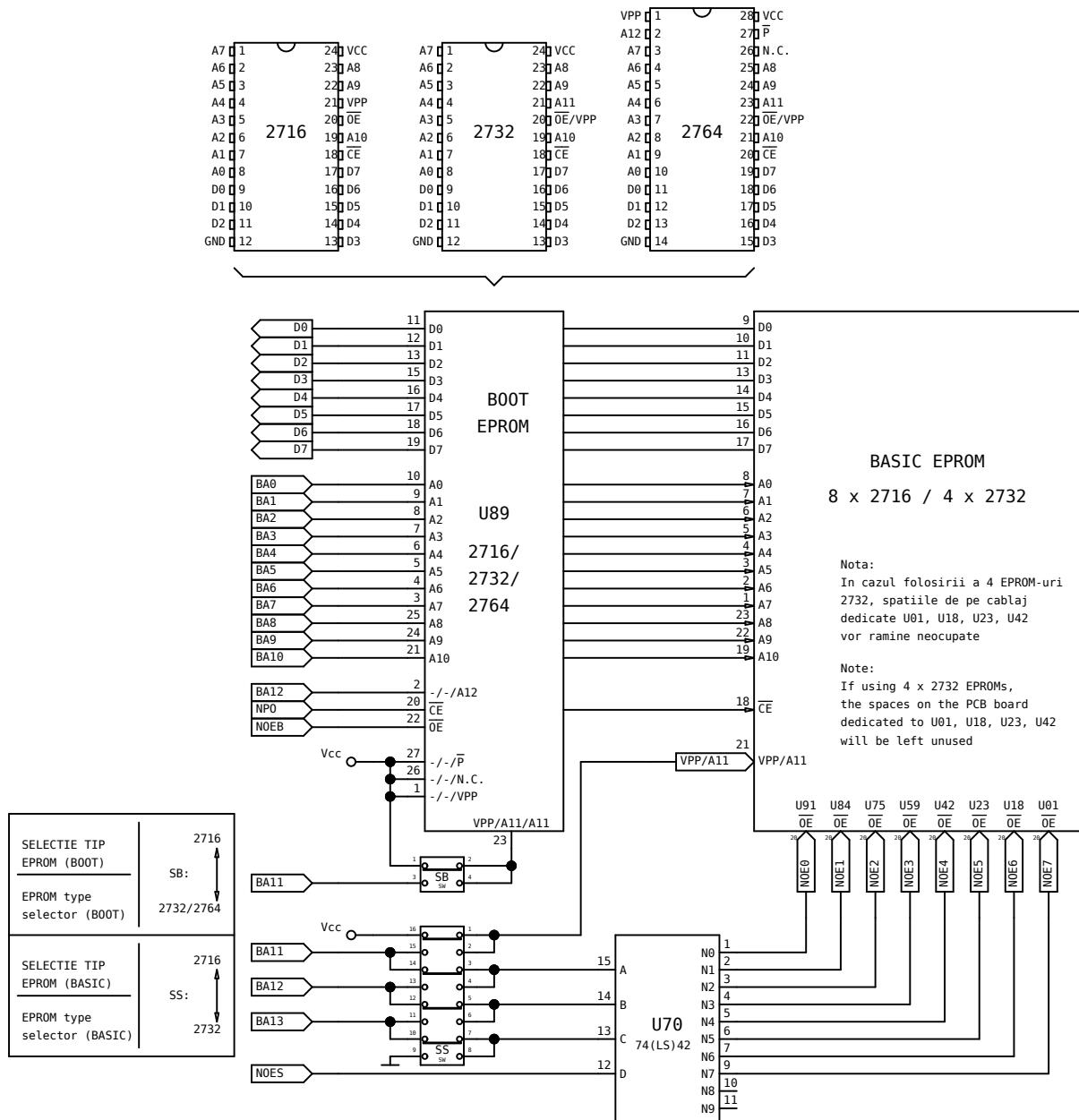
FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

PAGE 9 OF 16

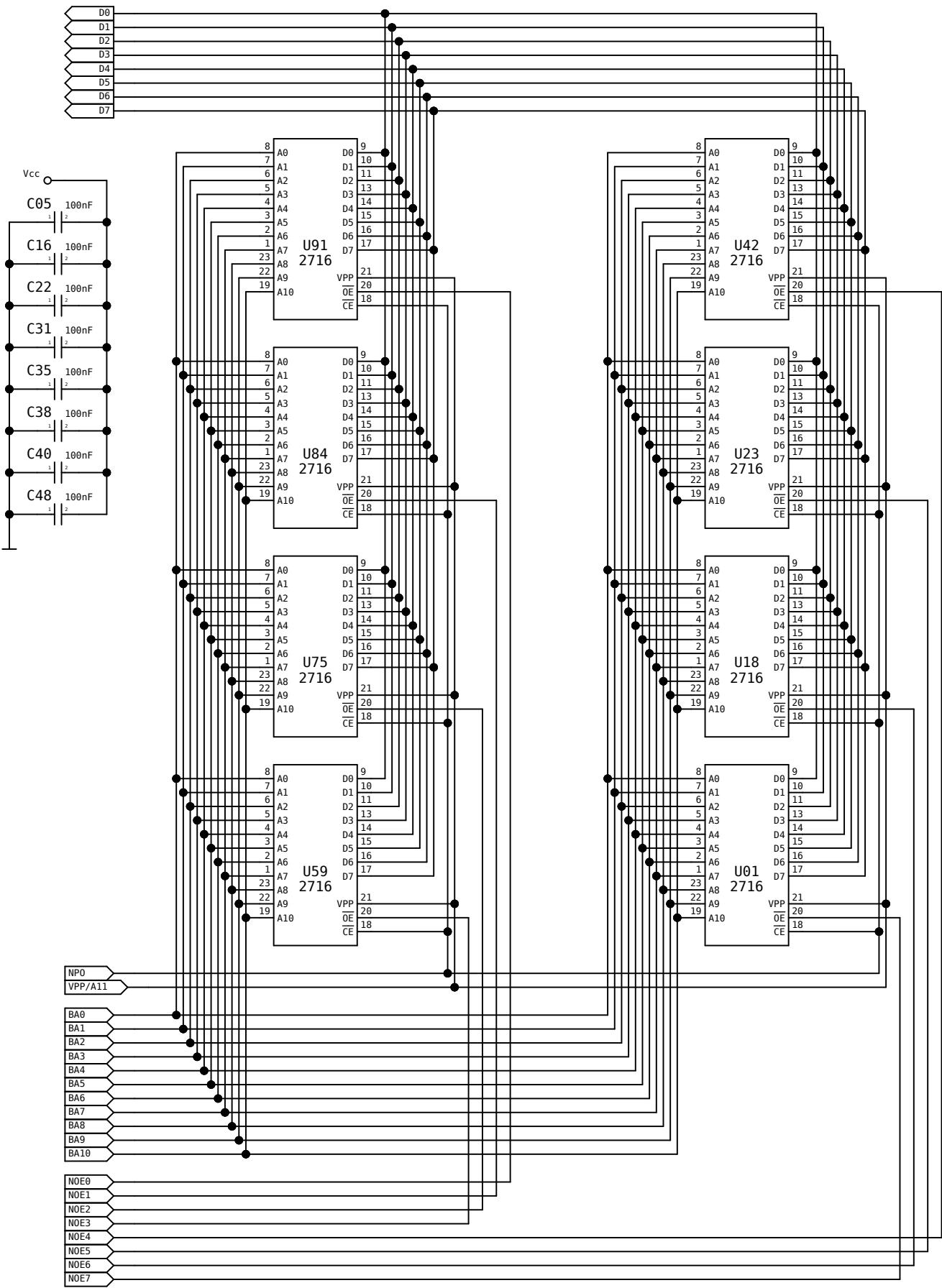
DRAWN BY: ElectroNNix





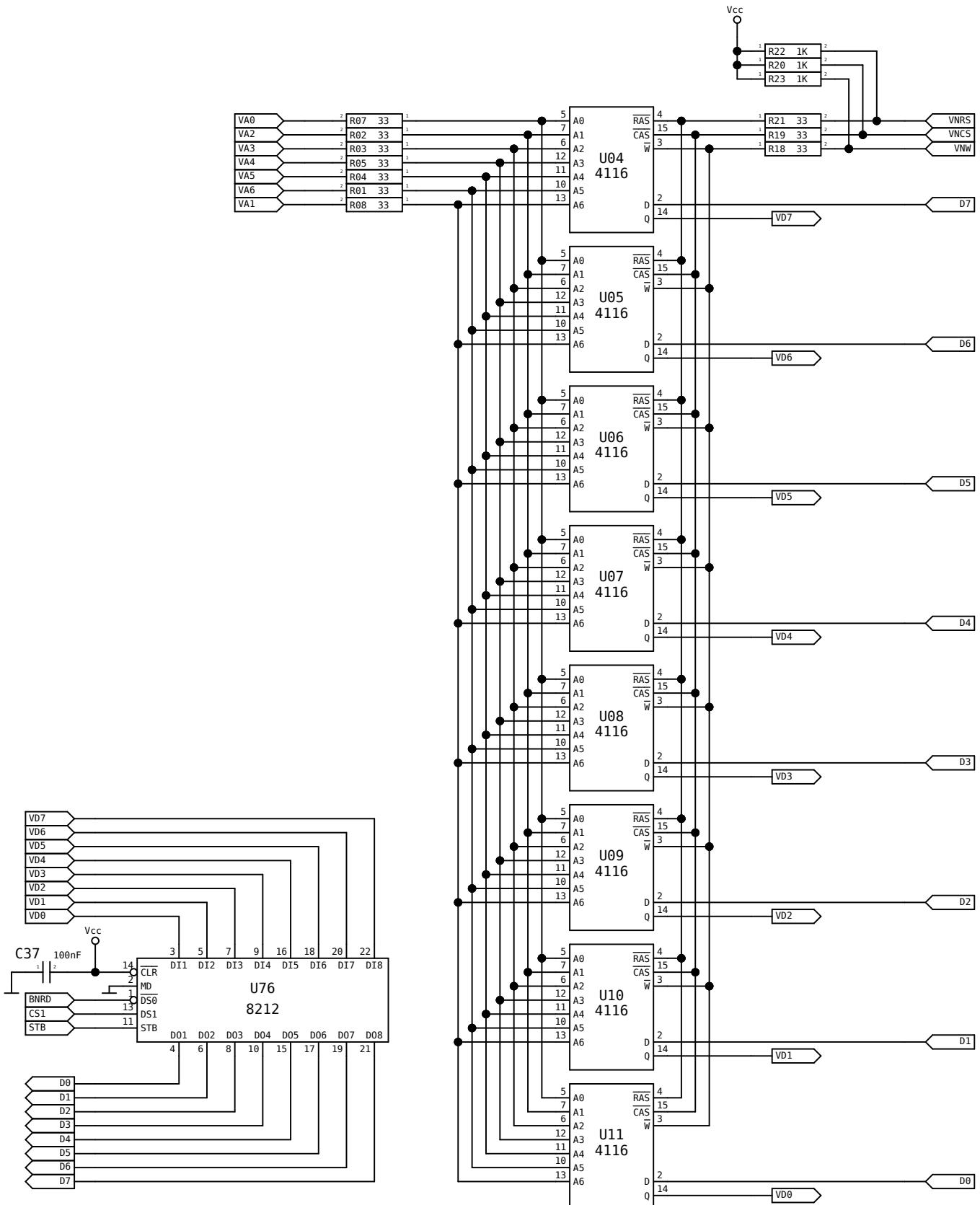
TITLE µC CoBra - Circuitul memoriei nevolatile - pag.1/2
CoBra µC - Read-only memory circuit - pag.1/2

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 10 OF 16	DRAWN BY: ElectroNNix



TITLE µC CoBra - Circuitul memoriei nevolatile - pag.2/2
CoBra µC - Read-only memory circuit - pag.2/2

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 11 OF 16	DRAWN BY: ElectroNNix



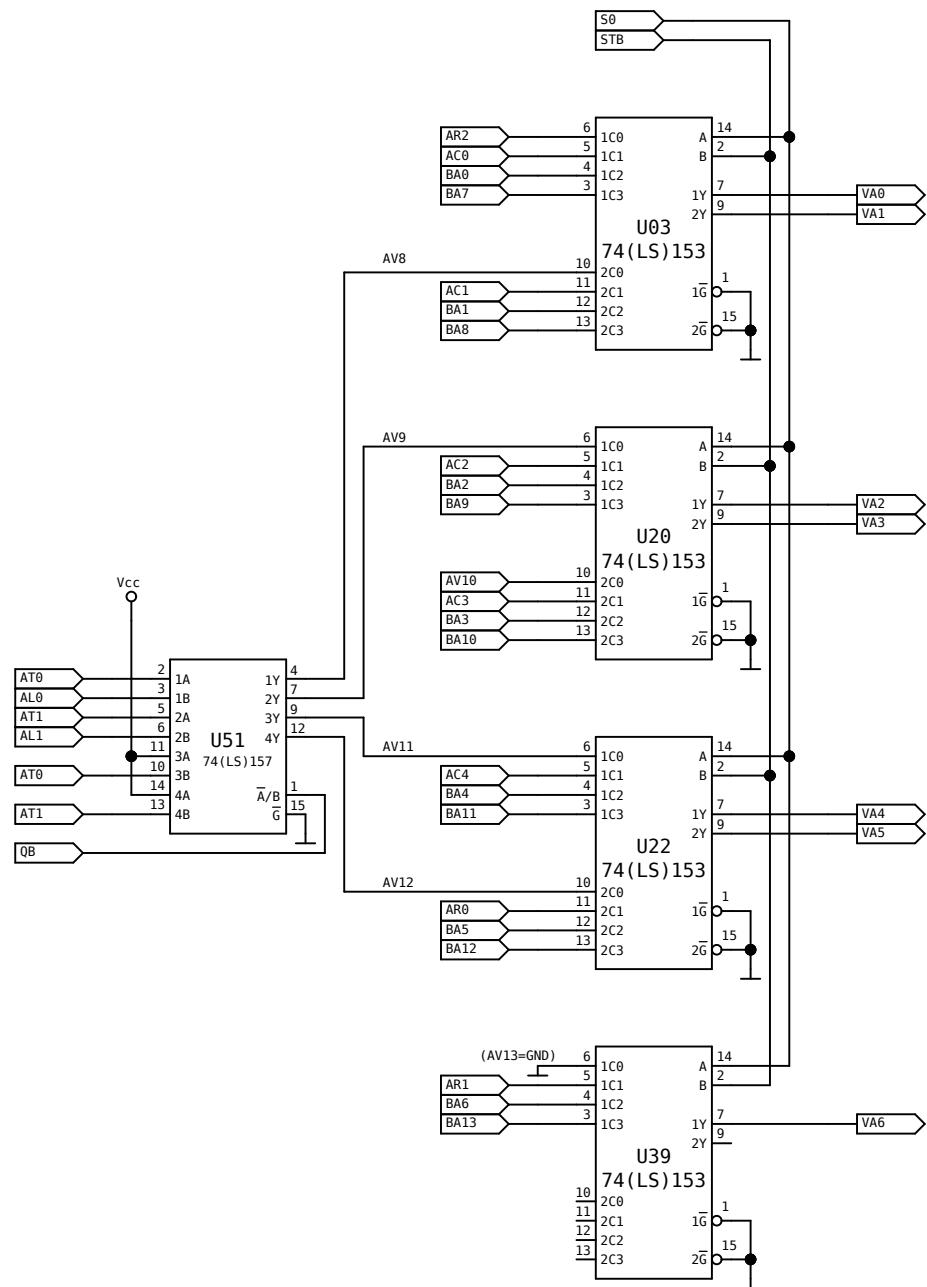
TITLE **μ C CoBra - Circuitul memoriei video**
CoBra μ C - Video memory circuit

FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

PAGE 12 OF 16

DRAWN BY: ElectroNNix

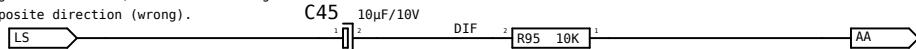


TITLE μC CoBra - Circuitul de multiplexare adrese video	
CoBra μC - Video address multiplexer circuit	

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 13 OF 16	DRAWN BY: ElectroNNix

* (1) In schema originala semnalele LS si AA erau desenate in sens opus (gresit).

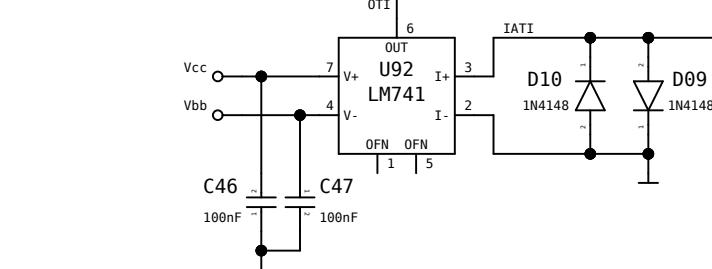
* (1) In the original schematics, the LS and AA signals were drawn in opposite direction (wrong).



* (2) In schema originala dioda D08*

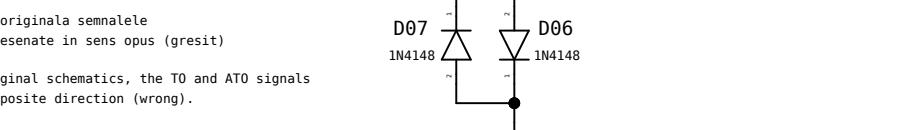
nu avea nume, iar pe cablajul original nu era prevazuta. Am modificat cablajul adaugind loc pentru dioda.

* (2) In the original schematics, diode D08* was not named, and it was not placed on the original mainboard. I have modified the mainboard by adding mounting holes for the diode.



* (3) In schema originala semnalele T0 si ATO erau desenate in sens opus (gresit)

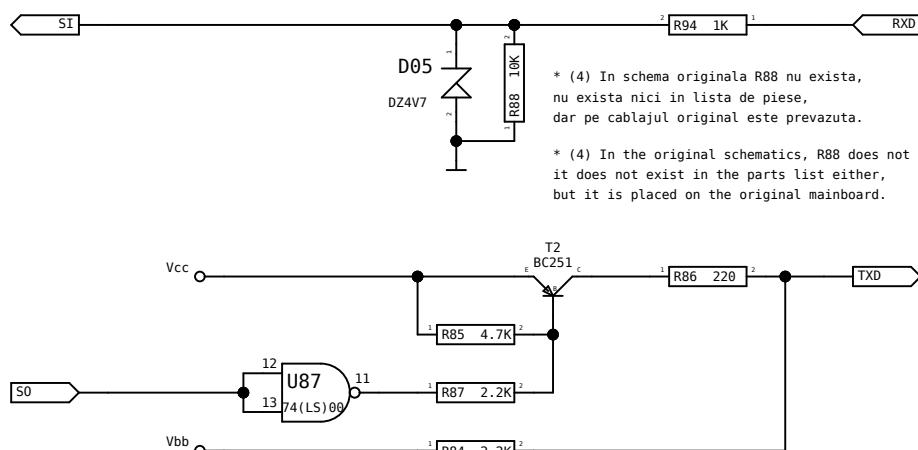
* (3) In the original schematics, the T0 and ATO signals were drawn in opposite direction (wrong).



* (4) In schema originala R88 nu exista,

nu exista nici in lista de piese,
dar pe cablajul original este prevazuta.

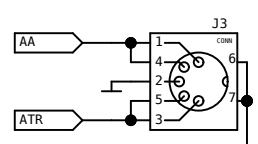
* (4) In the original schematics, R88 does not exist, it does not exist in the parts list either, but it is placed on the original mainboard.



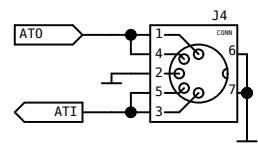
* (5) Pe cablajul original, poarta U87/13,12,11 era intercalata ca inversor intre U85/12 si U86/11, inversand semnalul I de la U85 la U86 (gresit). Am modificat deci cablajul conform acestei scheme (originale, corecte). (Vezi taiteturile #1 si #2 de pe fata 1, #20 si #24 de pe fata 2, si legaturile #18, #20 si #21 de pe fata 2)

* (5) On the original PCB, gate U87/13,12,11 was placed as inverter between U85/12 and U86/11, inverting the signal I from U85 to U86 (wrong). I have therefore changed the mainboard layout according to the original (correct) schematic (shown here). (See cuts #1 & #2 on side 1, #20 & #24 on side 2, and rewirings #18, #20 & #21 on side 2)

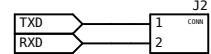
J3 - CONECTOR AUXILIAR
J3 - AUX CONNECTOR



J4 - CONECTOR CASETOFON
J4 - TAPE CONNECTOR



J2 - CONECTOR RS232
J2 - RS232 CONNECTOR



TITLE µC CoBra - Circuite de adaptare nivel
CoBra µC - Voltage-level adapter circuits

FILE: CoBra

REVISION: 3 (original design, 64KB DRAM)

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DRAWN BY: ElectroNNix

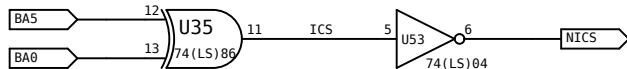
* (1) Pe cabajul original JEXA/8 este legat in mod gresit la BA7.

De asemenea, manualul original avea JEXA/8 listat ca fiind

legat la BA7. Am modificat deci cabajul si

schema de fata legind JEXA/8 la BA1 (corect).

(Vesti tajetura #11 fata 1, legatura #22 fata 2)



* (1) On the original mainboard, JEXA/8 was connected

(the wrong way) to BA7. Also the original hardware

manual had JEXA/8 listed as being connected to BA7.

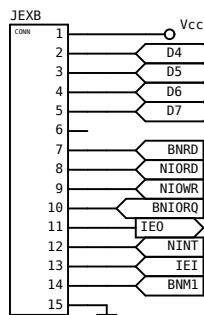
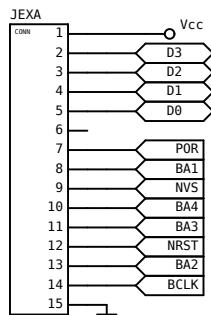
I have therefore changed the mainboard layout

and this schematic by connecting JEXA/8 to BA1 (correctly).

(See cut #11 side 1, rewiring #22 side 2)

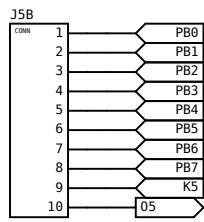
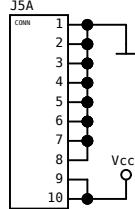
JEXA+B - CONECTOR INTERFATA FLOPPY DISK

JEXA+B - FLOPPY DISK INTERFACE CONNECTOR



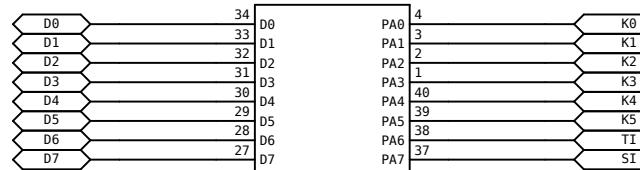
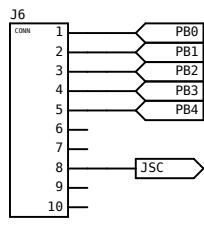
J5A+B - CONECTOR PORT INTRARE PE 8 BITI ADRESA 0DFH

J5A+B - 8-BIT INPUT PORT 0DFH CONNECTOR



J6 - CONECTOR JOYSTICK KEMPSTON

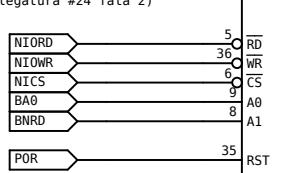
J6 - KEMPSTON JOYSTICK CONNECTOR



* (2) Pe cabajul original JEXA/9 era legat la o via care nu ducea nicaieri mai departe.

In schema originale JEXA/9 era legat la un semnal SI/TRG3 care nu exista nicaieri in alta parte. Pe placă mea funcțională JEXA/9 este legat la NVS.

(Vesti legatura #24 fata 2)

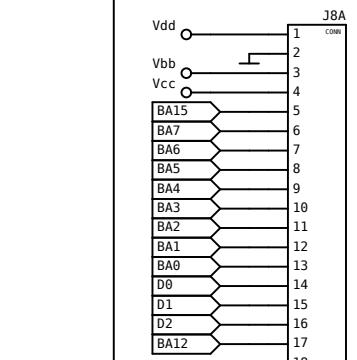
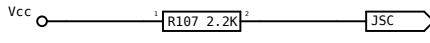


* (2) On the original mainboard, JEXA/9 was connected to a via which was not further leading anywhere.

In the original schematics, JEXA/9 was connected to a signal "SI/TRG3" which did not exist anywhere else.

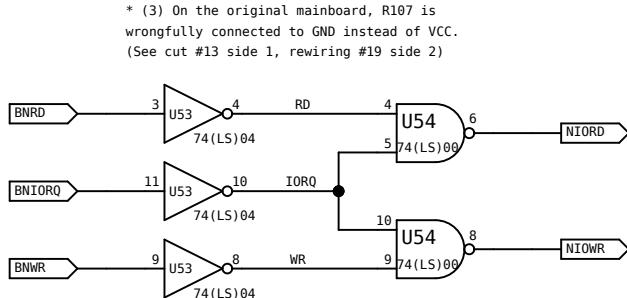
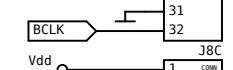
On my working mainboard, JEXA/9 is connected to NVS. (See rewiring #24 side 2)

* (3) Pe cabajul original, R107 este legata in mod gresit la GND in loc de VCC. (Vesti tajetura #13 fata 1, legatura #19 fata 2)



J8A+B+C - CONECTOR EXTENSIE

J8A+B+C - EXPANSION CONNECTOR



* (4) Cabajul original avea JSC conectat la J6/pin10 dar manualul original avea JSC listat la J6/pin8. Am schimbat cabajul placii de baza pentru a corespunde manualului.

(Vesti tajetura #5 fata 1, legatura #1 fata 1)

* (4) The original mainboard had JSC connected to J6/pin10 but the original manual had JSC listed at J6/pin8. I changed the mainboard layout to match the original manual.

(See cut #5 side 1, rewiring #1 side 1)

TITLE μC CoBra - Interfete CoBra μC - Interfaces

FILE: CoBra

REVISION:

3 (original design, 64KB DRAM)

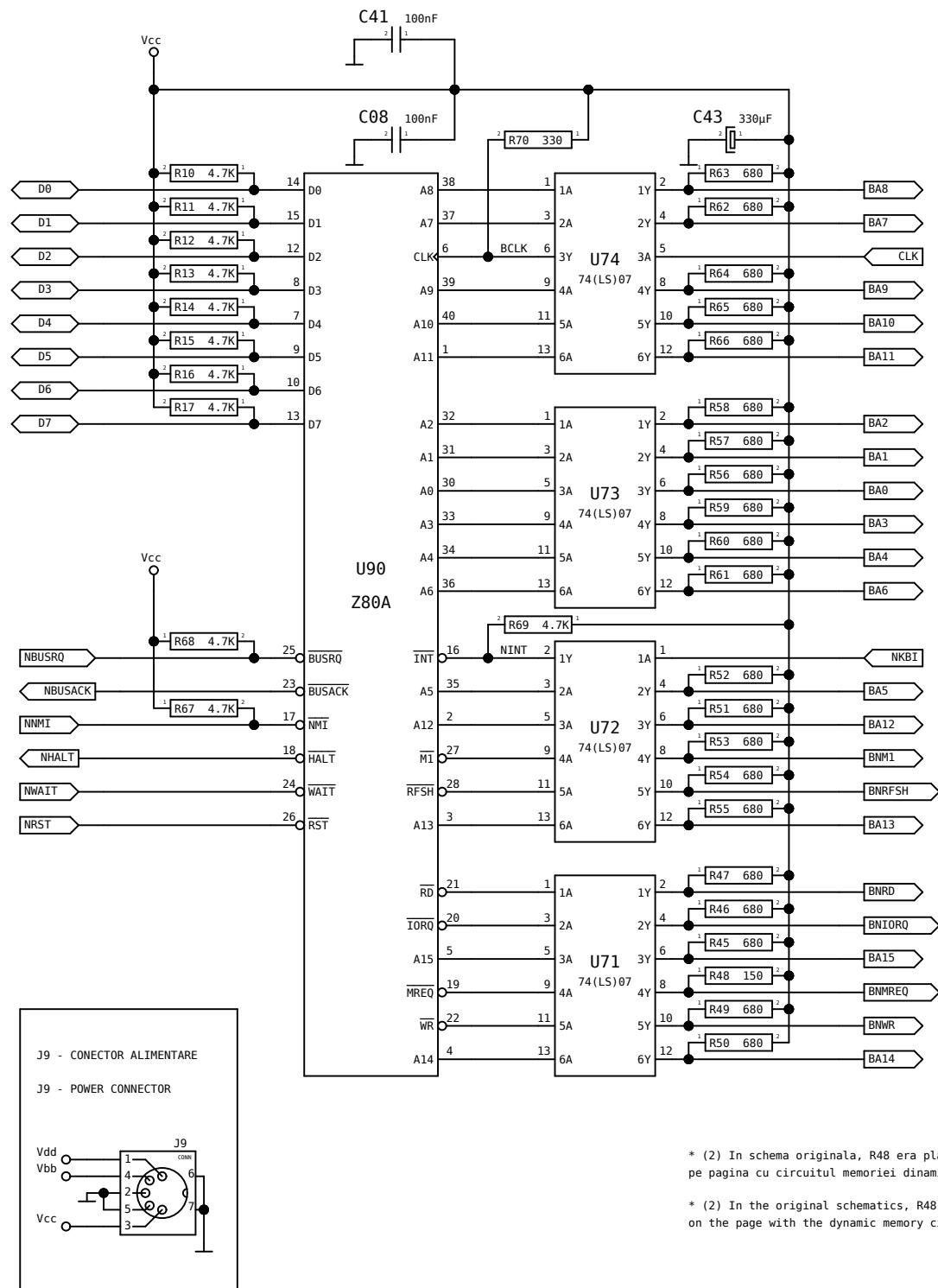
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DRAWN BY:

ElectroNNix

* (1) In schema originala, U74/6 era legat (gresit) la U90/24, dar corect este ca U90/24 sa fie legat la NWAIT, U74/6 (BCLK) sa fie legat la U90/6 (CLK procesor) si U74/5 sa fie legat la CLK

* (1) In the original schematics, U74/6 was connected (wrong) to U90/24, but correct is for U90/24 to be connected to NWAIT, for U74/6 (BCLK) to be connected to U90/6 (CPU clock) and for U74/5 to be connected to CLK



TITLE µC CoBra - Unitatea centrală
CoBra µC - Central Processing Unit

FILE: CoBra	REVISION: 3 (original design, 64KB DRAM)
PAGE 16 OF 16	DRAWN BY: ElectroNNix